

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises a cell array
5 including bit lines arranged at a uniform pitch; and a
plurality of bit line selection transistors connected to
respective bit line ends for selectively connecting the bit
line to a sense amp. The bit line selection transistors
are translationally arrayed in a direction perpendicular to
10 the bit line at an average array pitch greater than eight
times the pitch of the bit lines.